

Notice of References Cited	Application/Control No. 10/736,326	Applicant(s)/Patent Under Reexamination GOIKE ET AL.	
	Examiner Vuthe Siek	Art Unit 2825	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-6,449,762	09-2002	McElvain, Kenneth S.	716/18
	C	US-6,904,571	06-2005	Schmidt et al.	716/2
	D	US-5,463,563	10-1995	Bair et al.	716/11
	E	US-6,311,316	10-2001	Huggins et al.	716/12
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	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Naveen et al., "AN AUTOMACTIC NETLIST-TO-SCHEMATIC GENERATOR," IEEE, 1993, pp. 36-41.
	V	Kim et al., "RIGHT TOPOLOGIZER: AN EFFICIENT SCHEMATIC GENERATOR FOR MULTI-LEVEL OPTIMIZATION," IEEE, 2000, PP. 387-391.
	W	Hutchings et al., "DEVELOPING AND DEBUGGING FPGA APPLICATIONS IN HARDWARE WITH JHDL," IEEE, 1999, PP. 554-558.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.